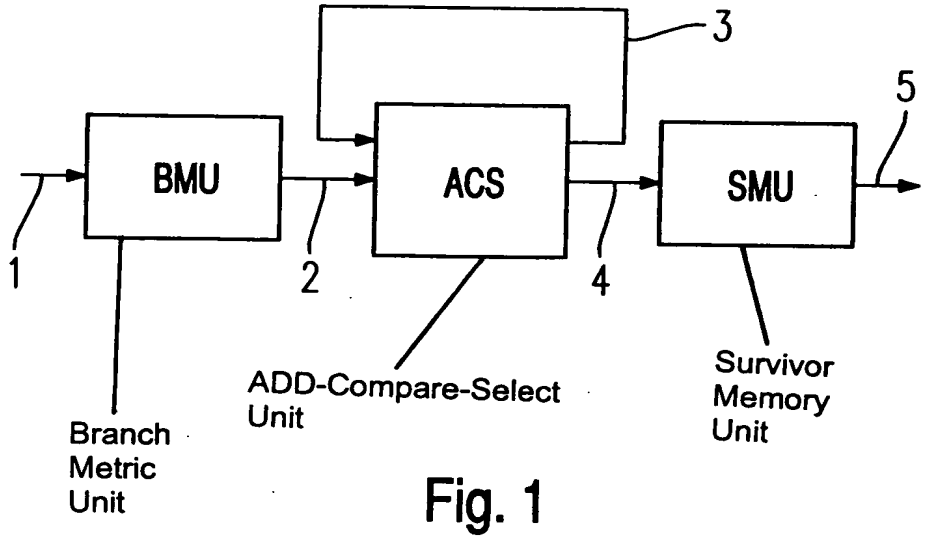
3
5
BMU
ACS
SMU
1
2
4
Branch
Metric
Unit
ADD-Compare-Select
Unit
Survivor
Memory
Unit

Fig. 1

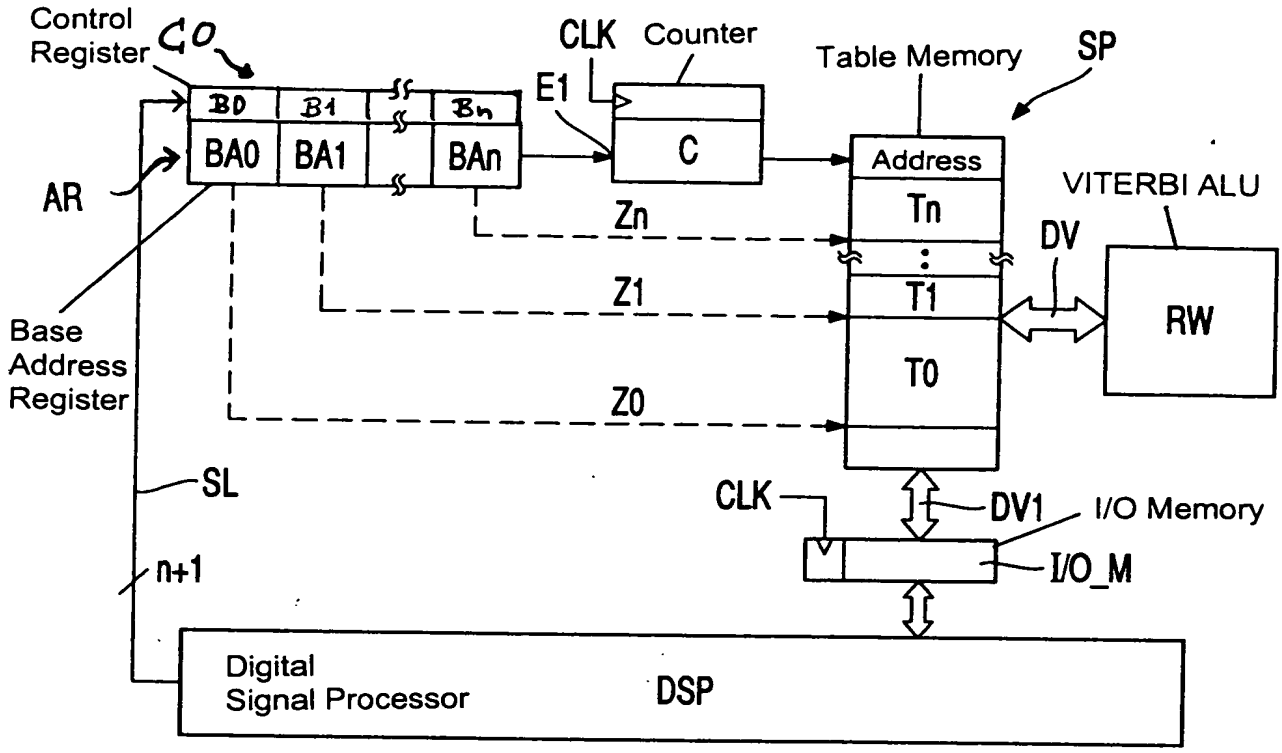
Control Register
CO
CLK
Counter
Table Memory
SP
E1
B0
B1
Bn
BA0
BA1
BAn
C
Address
Tn
T1
T0
AR
Zn
Z1
Z0
VITERBI ALU
DV
RW
Base Address Register
SL
CLK
DV1
I/O Memory
I/O_M
n+1
Digital Signal Processor
DSP

Fig. 2

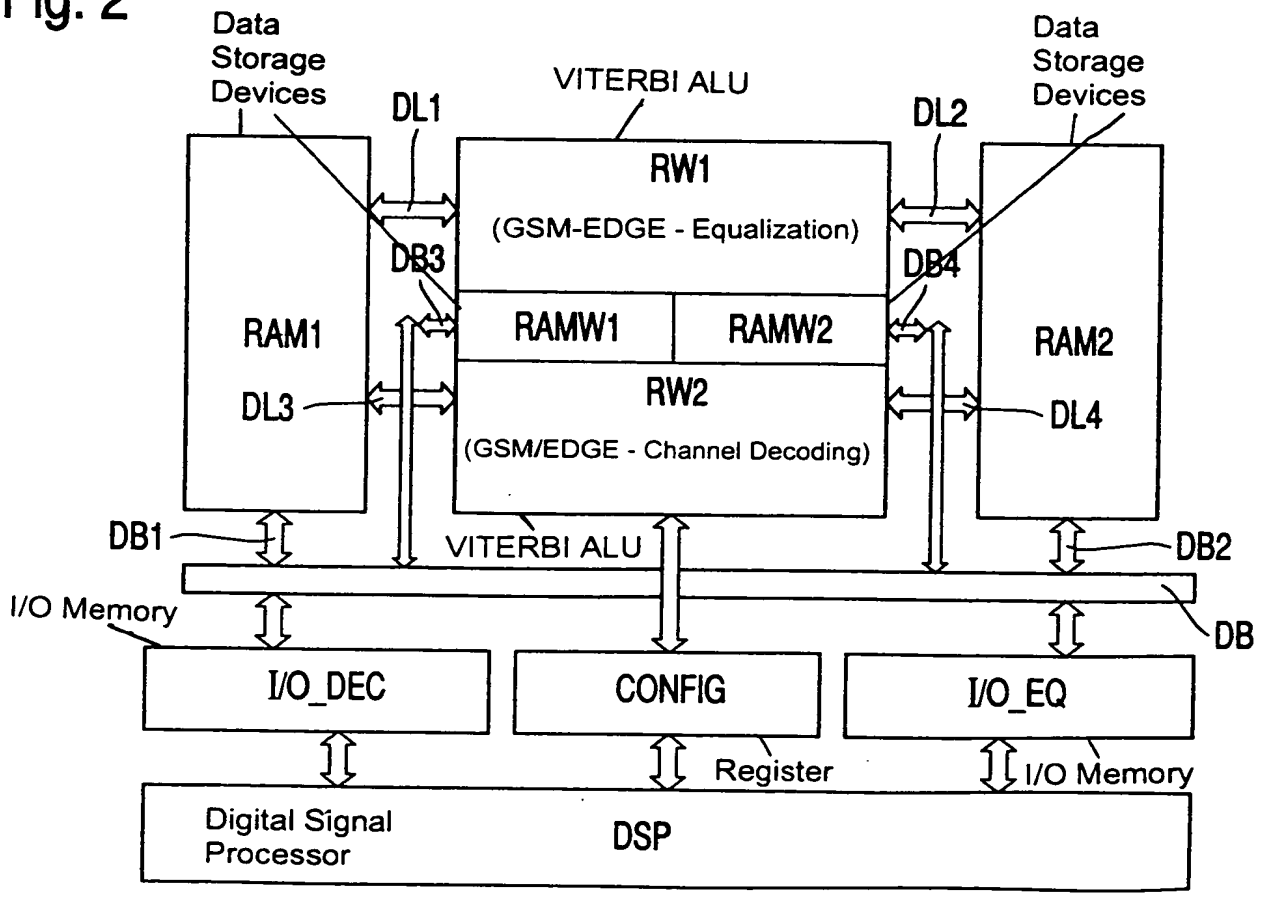
Data Storage Devices
DL1
VITERBI ALU
DL2
Data Storage Devices
RW1
(GSM-EDGE - Equalization)
DB3
DB4
RAM1
RAMW1
RAMW2
RAM2
DL3
RW2
DL4
(GSM/EDGE - Channel Decoding)
DB1
VITERBI ALU
DB2
I/O Memory
DB
I/O_DEC
CONFIG
I/O_EQ
Register
I/O Memory
Digital Signal Processor
DSP

Fig. 3

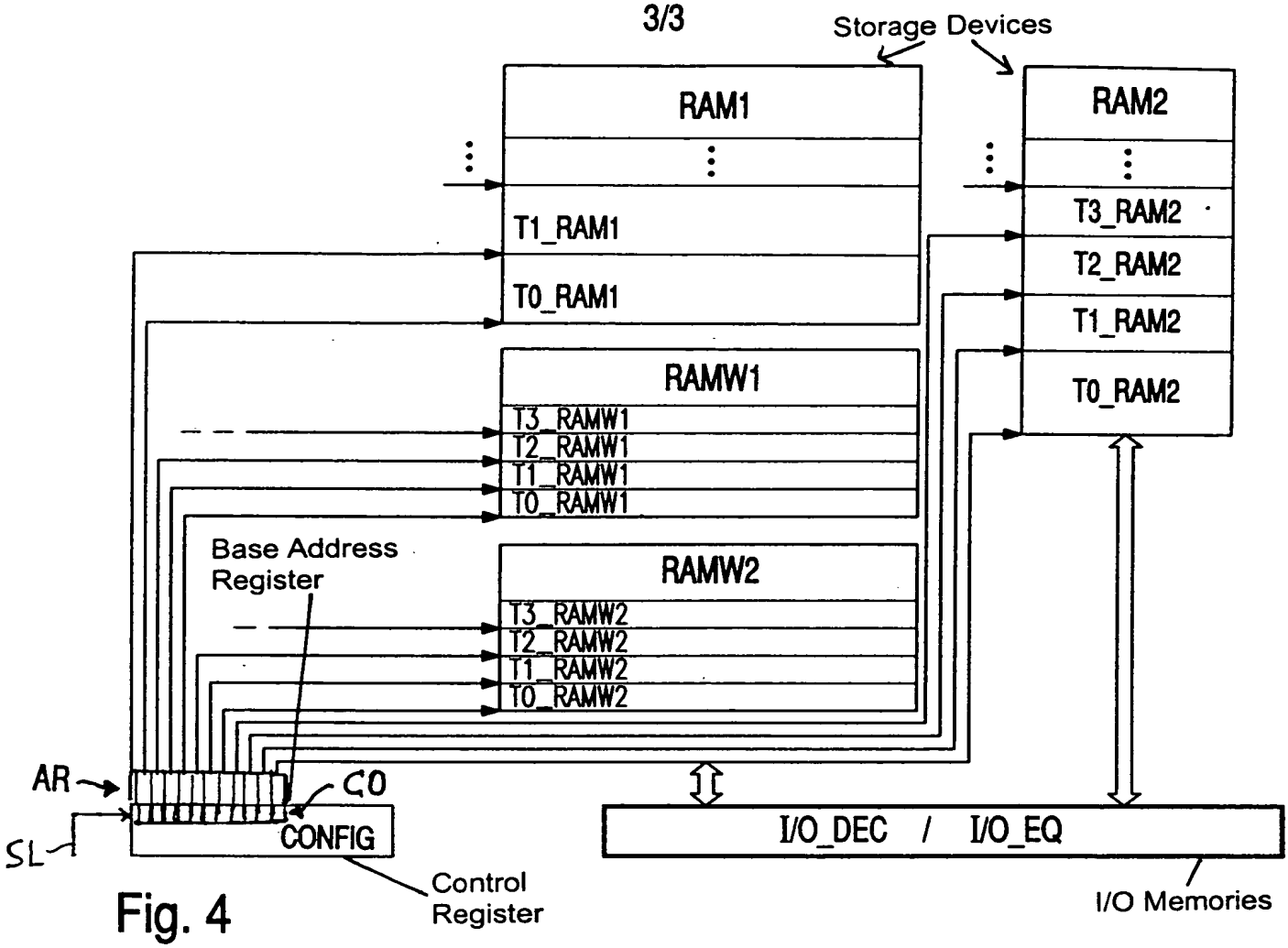
Storage Devices
RAM1
T1_RAM1
T0_RAM1
RAM2
T3_RAM2
T2_RAM2
T1_RAM2
T0_RAM2
RAMW1
T3_RAMW1
T2_RAMW1
T1_RAMW1
T0_RAMW1
RAMW2
T3_RAMW2
T2_RAMW2
T1_RAMW2
T0_RAMW2
Base Address Register
AR
CO
SL
CONFIG
Control Register
I/O_DEC / I/O_EQ
I/O Memories

Fig. 4

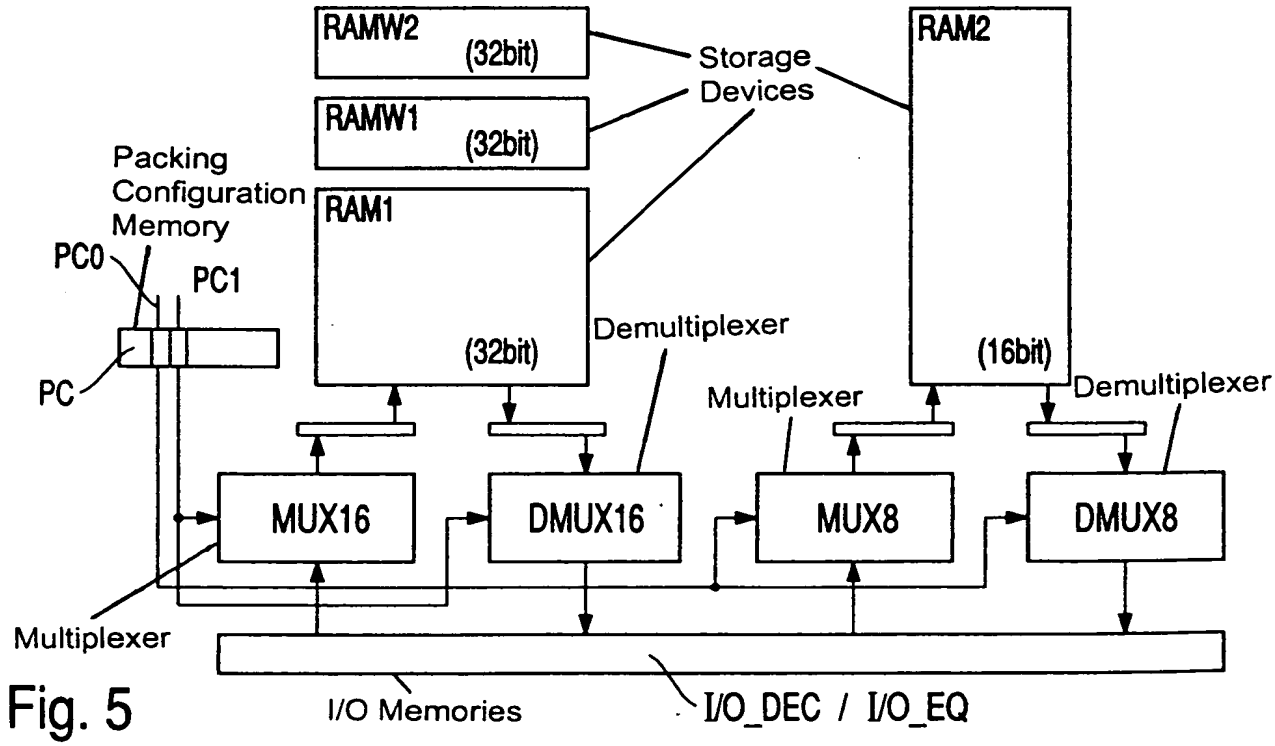
RAMW2 (32bit)
RAMW1 (32bit)
RAM1 (32bit)
RAM2 (16bit)
Storage Devices
Packing Configuration Memory
PC0
PC1
PC
Demultiplexer
Multiplexer
Demultiplexer
MUX16
DMUX16
MUX8
DMUX8
Multiplexer
I/O Memories
I/O_DEC / I/O_EQ

Fig. 5